I CLAIM:

1. A method for modeling a semiconductor device comprising the steps of:
(a) modeling the semiconductor device with a semiphysical model;
(b) modeling the semiconductor device with an analytical thermal model; and
(c) coupling the semi-physical model and said analytical conduction model.

2. The method as recited in claim 1, further including step (d) determining the internal charge/electric field structure of the semiconductor device.

3. The method as recited in claim 1, wherein said semi-physical model is configured to replicate measured direct current (DC) current-voltage (I-V) characteristics.

4. The method as recited in claim 3, wherein said semi-physical model is also configured to replicate bias dependent small signal characteristics.

5. the method as recited in claim 4, wherein said semi-physical model is configured to replicate said DC I-V and bias dependent.

6. The method as recited in claim 1, wherein step (b) includes the step (e): measuring the DC-IV characteristics and the S-parameter small signal parameters across a predetermined range of temperatures.

7. The method as recited in claim 6, further including the step (f): extracting small signal equivalent circuit models for each S-parameter measurement as a function of temperature.

8. The method as recited in claim 7, further including step (g): developing temperature co-efficient which adjust the semi-physical device model to match the measured DC and S-parameter measurements at each temperature.

9. The method as recited in claim 1, wherein step (c) includes the step (h): substituting the environment temperature that operates in any temperature dependent terms and temperature co-efficient with the channel temperature of the device.

10. The method as recited in claim (a), wherein step (c) further includes step (i): using of the saturated region as the length of the heat generating region.